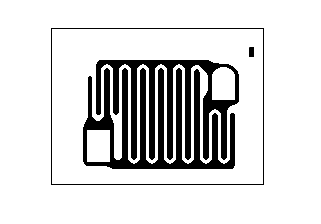
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.021”**



**.0015” RADIUS**

**D**

**S**

**.016”**

**.003 X .004”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: S = .003” X .004” D = .0015”**

**Backside Potential: Gate**

**Mask Ref: 5001**

**APPROVED BY: DK DIE SIZE .016” X .021” DATE: 10/20/21**

**MFG: CALOGIC THICKNESS .018” P/N: 2N4391**

**DG 10.1.2**

#### Rev B, 7/19/02